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(54) **ORGANIC LIGHT-EMITTING DISPLAY DEVICE AND DRIVING METHOD THEREOF**

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(57) **ABSTRACT**

An organic light-emitting display device is provided. The organic light-emitting display device comprises a substrate, a thin-film transistor (TFT) disposed on the substrate, an overcoat layer disposed on the TFT, a first electrode disposed on the overcoat layer and including a lower electrode layer, an intermediate electrode layer, which is disposed on the lower electrode layer, and an upper electrode layer, which is disposed on the intermediate electrode layer, an emission layer disposed on the first electrode, and a second electrode disposed on the emission layer, wherein the first electrode includes a first area in which the lower electrode layer, the intermediate electrode layer and the upper electrode layer are sequentially stacked and a second area in which the lower electrode layer and the upper electrode layer are sequentially stacked.

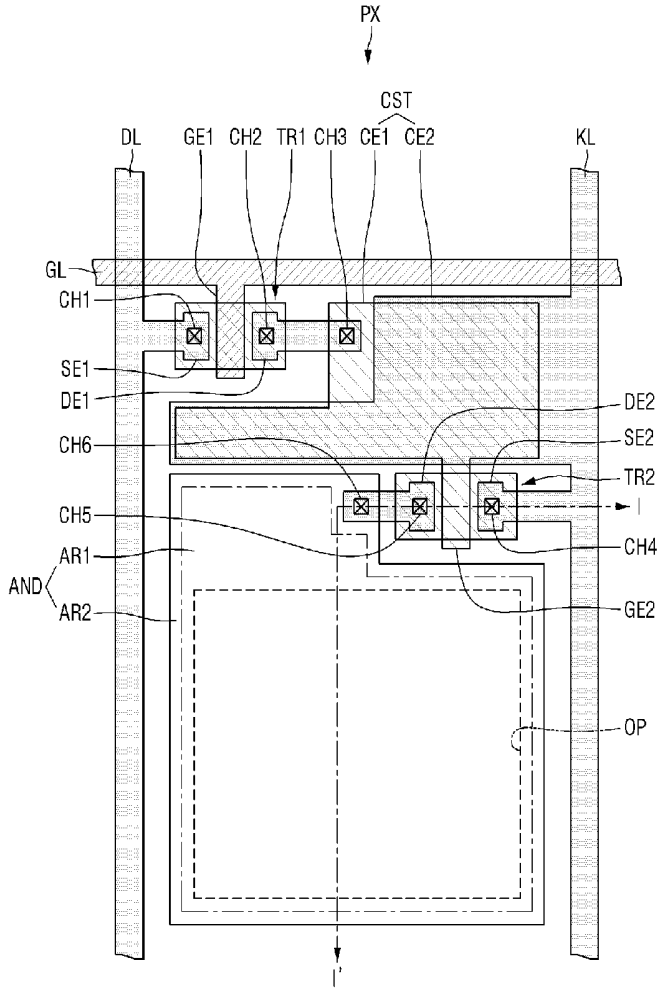


FIG.1

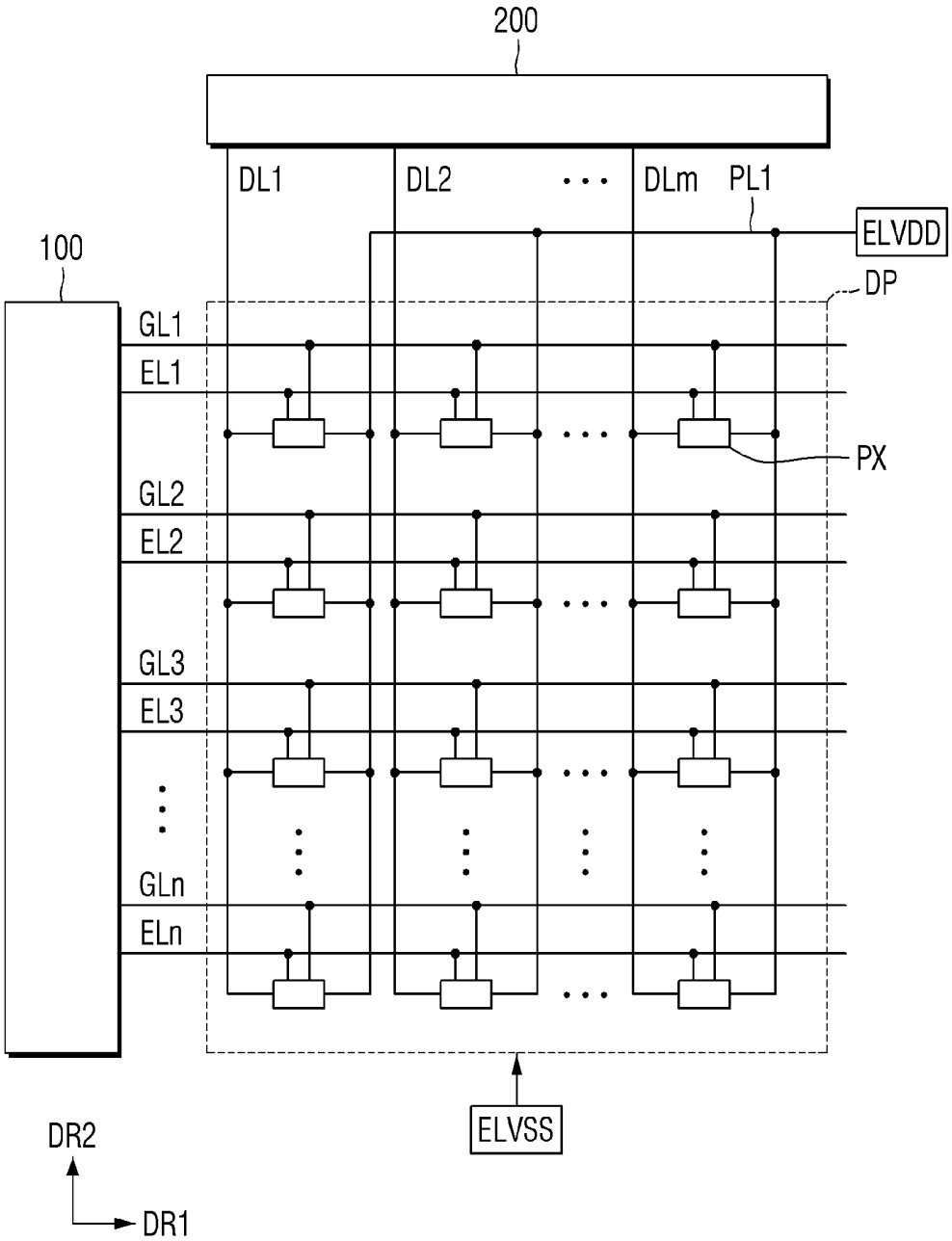

200
DL1
DL2
DLm
PL1
ELVDD
100
DP
GL1
EL1
PX
GL2
EL2
GL3
EL3
GLn
ELn
ELVSS
DR2
DR1

FIG.2

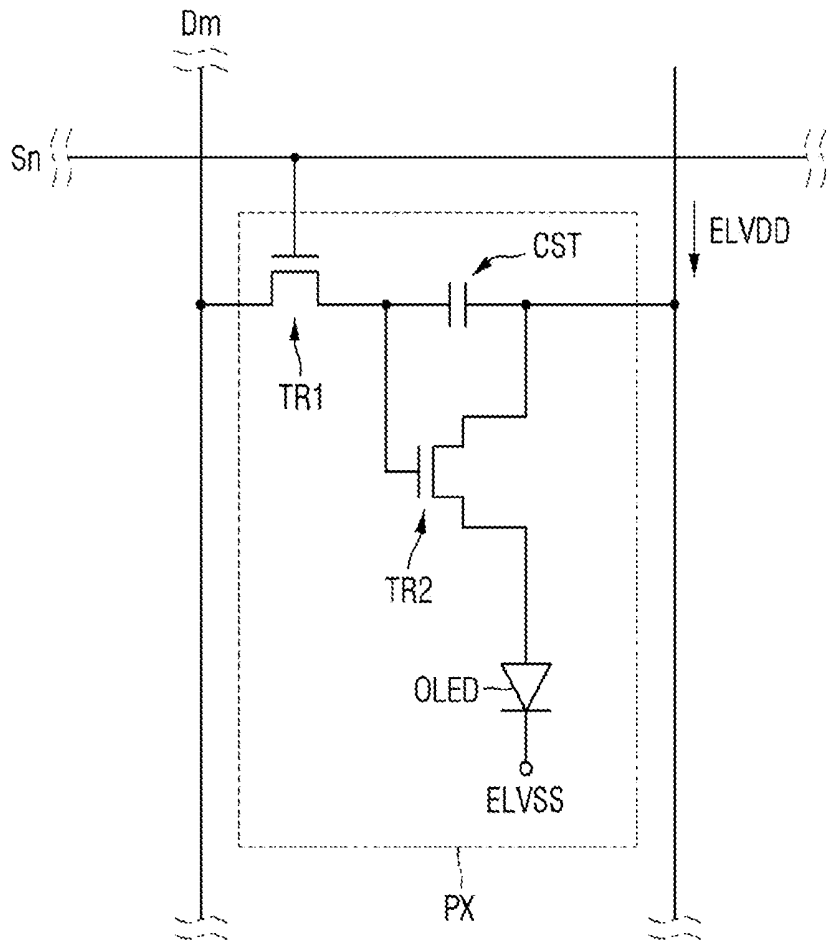


FIG.3

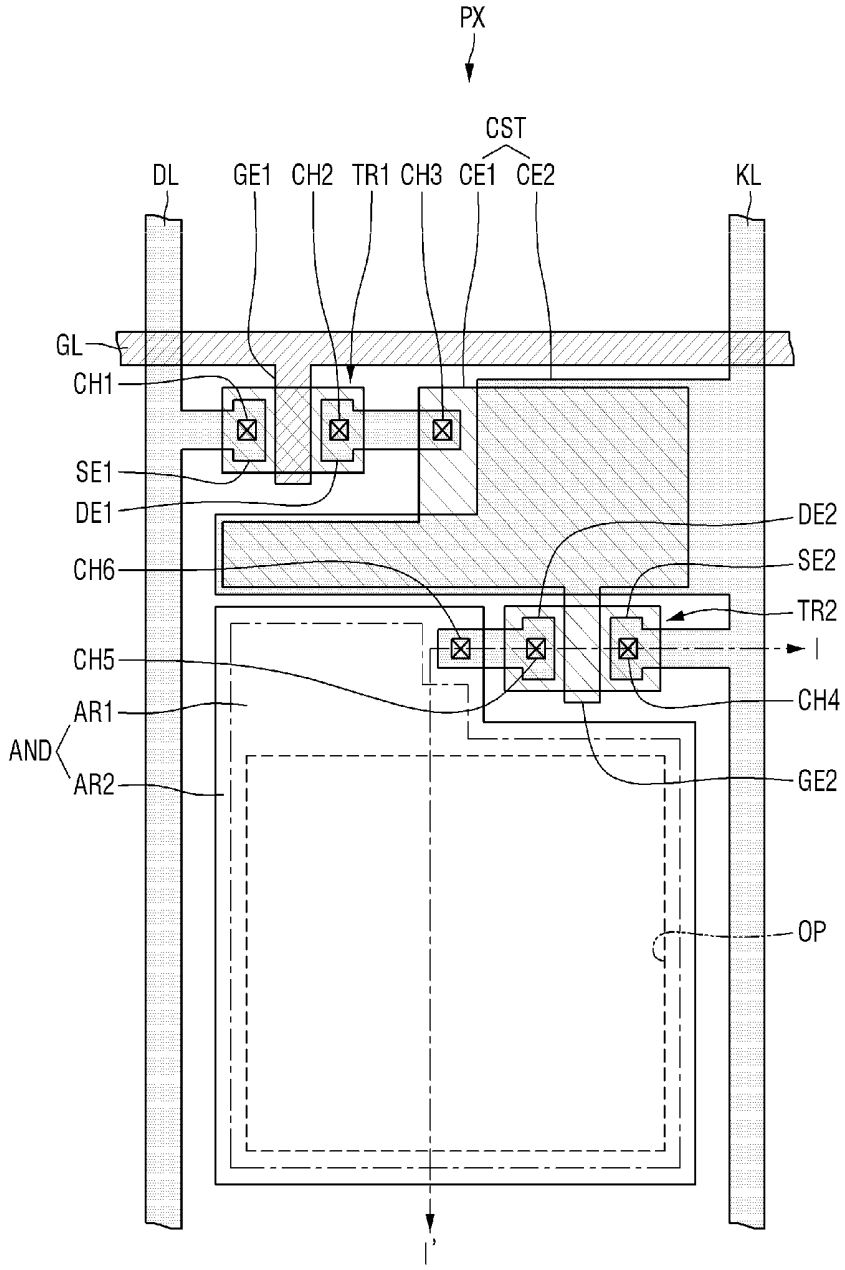

PX
CST
DL
GE1
CH2
TR1
CH3
CE1
CE2
KL
GL
CH1
SE1
DE1
CH6
CH5
AR1
AND
AR2
DE2
SE2
TR2
I
CH4
GE2
OP
I'

FIG.4

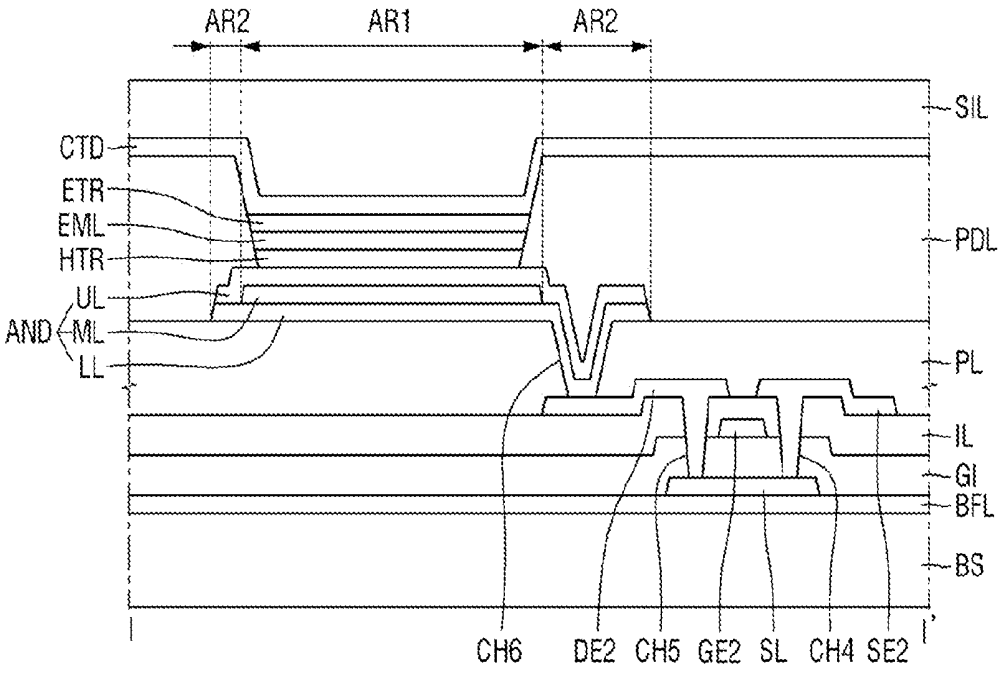
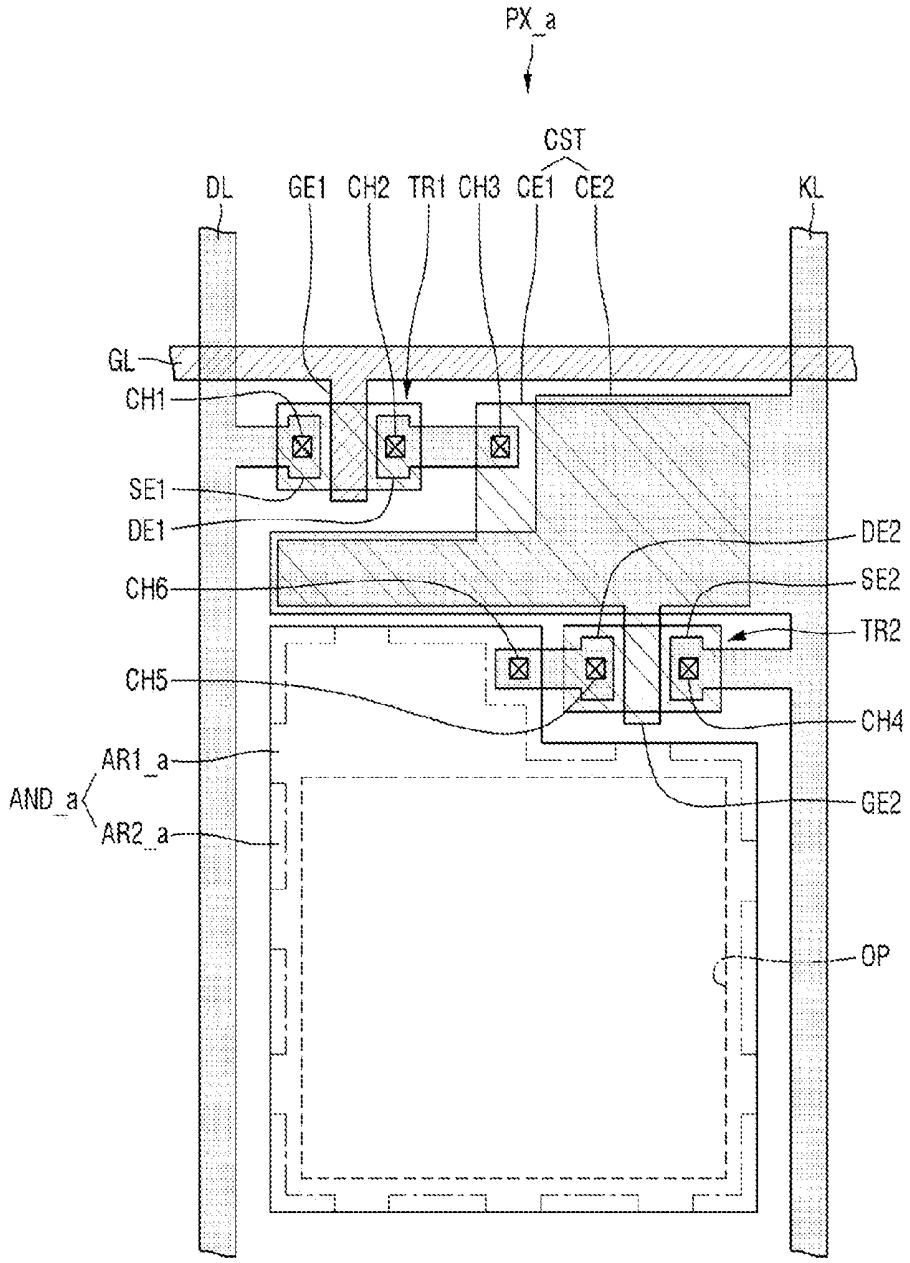

AR2
AR1
AR2
SIL
CTD
ETR
EML
HTR
PDL
UL
AND
ML
LL
PL
IL
GI
BFL
BS
I
CH6
DE2
CH5
GE2
SL
CH4
SE2
I'

FIG.5


PX_a
CST
DL
GE1
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TR1
CH3
CE1
CE2
KL
GL
CH1
SE1
DE1
CH6
CH5
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AND_a
AR2_a
DE2
SE2
TR2
CH4
GE2
OP

FIG.6

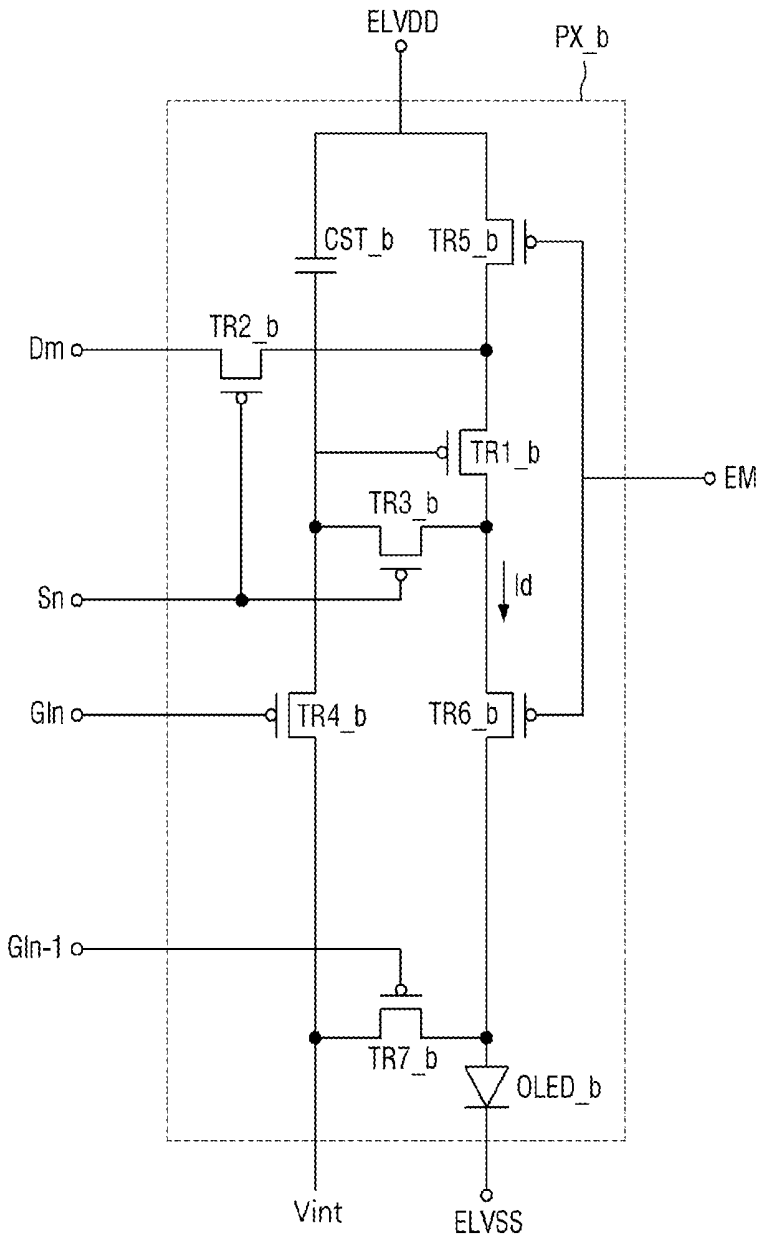
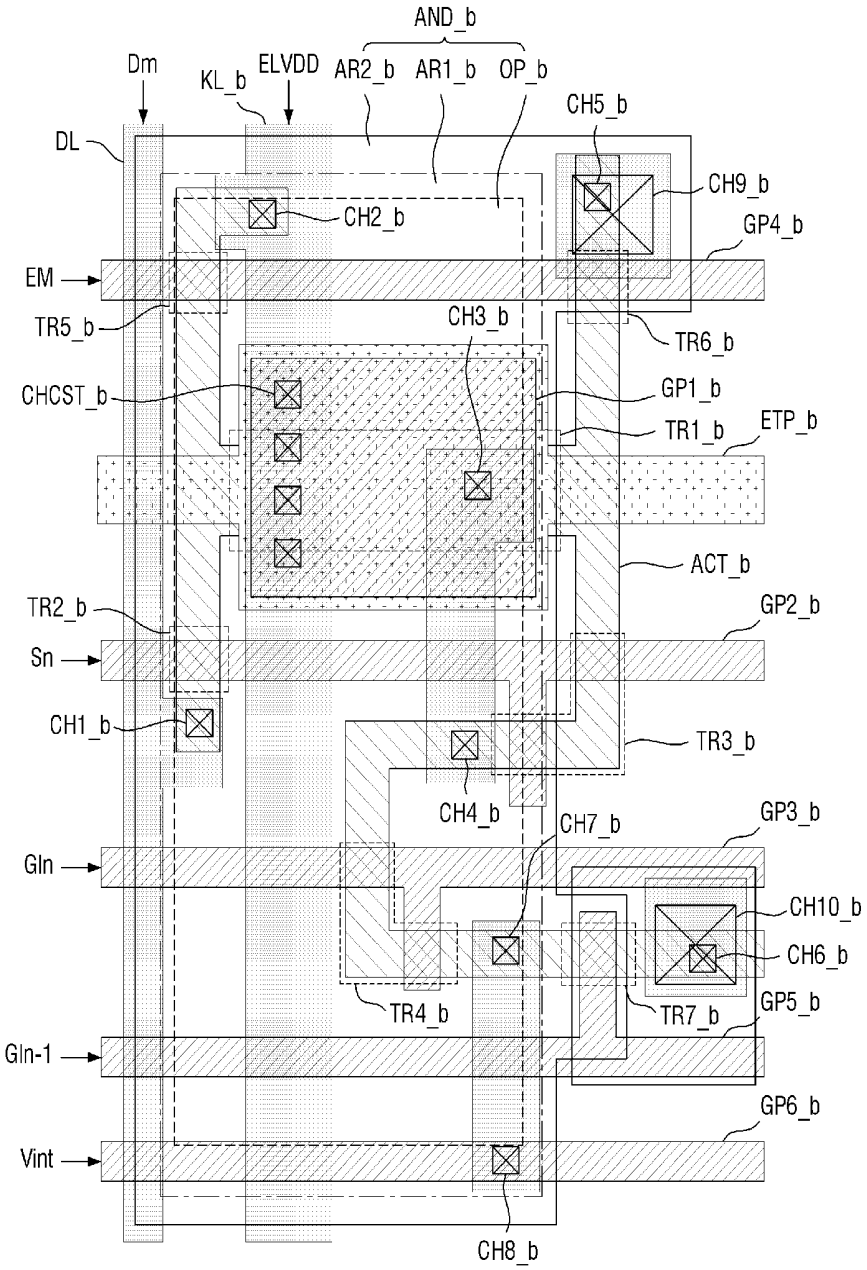

ELVDD
PX_b
CST_b
TR5_b
TR2_b
Dm
TR1_b
EM
TR3_b
Id
Sn
Gln
TR4_b
TR6_b
Gln-1
TR7_b
OLED_b
Vint
ELVSS

FIG.7


AND_b
Dm
KL_b
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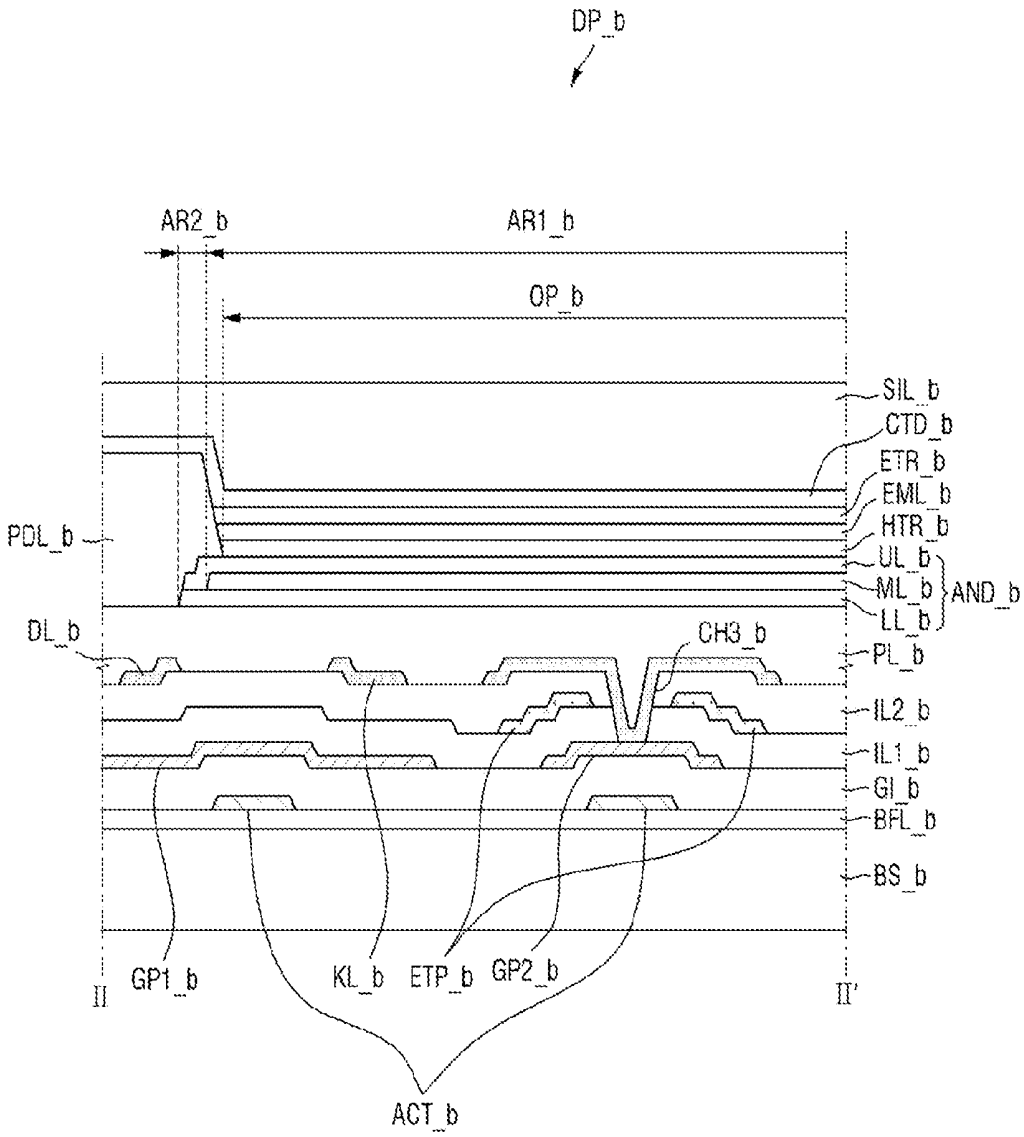
AR2_b
AR1_b
OP_b
CH5_b
DL
CH9_b
CH2_b
GP4_b
EM
TR5_b
CH3_b
TR6_b
CHCST_b
GP1_b
TR1_b
ETP_b
ACT_b
TR2_b
GP2_b
Sn
CH1_b
TR3_b
CH4_b
CH7_b
GP3_b
Gln
CH10_b
CH6_b
TR4_b
TR7_b
GP5_b
Gln-1
GP6_b
Vint
CH8_b

FIG.8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AR2_b
AR1_b
OP_b
SIL_b
CTD_b
ETR_b
EML_b
HTR_b
UL_b
ML_b
LL_b
AND_b
PDL_b
DL_b
CH3_b
PL_b
IL2_b
IL1_b
GI_b
BFL_b
BS_b
GP1_b
KL_b
ETP_b
GP2_b
II
II'
ACT_b

FIG.9

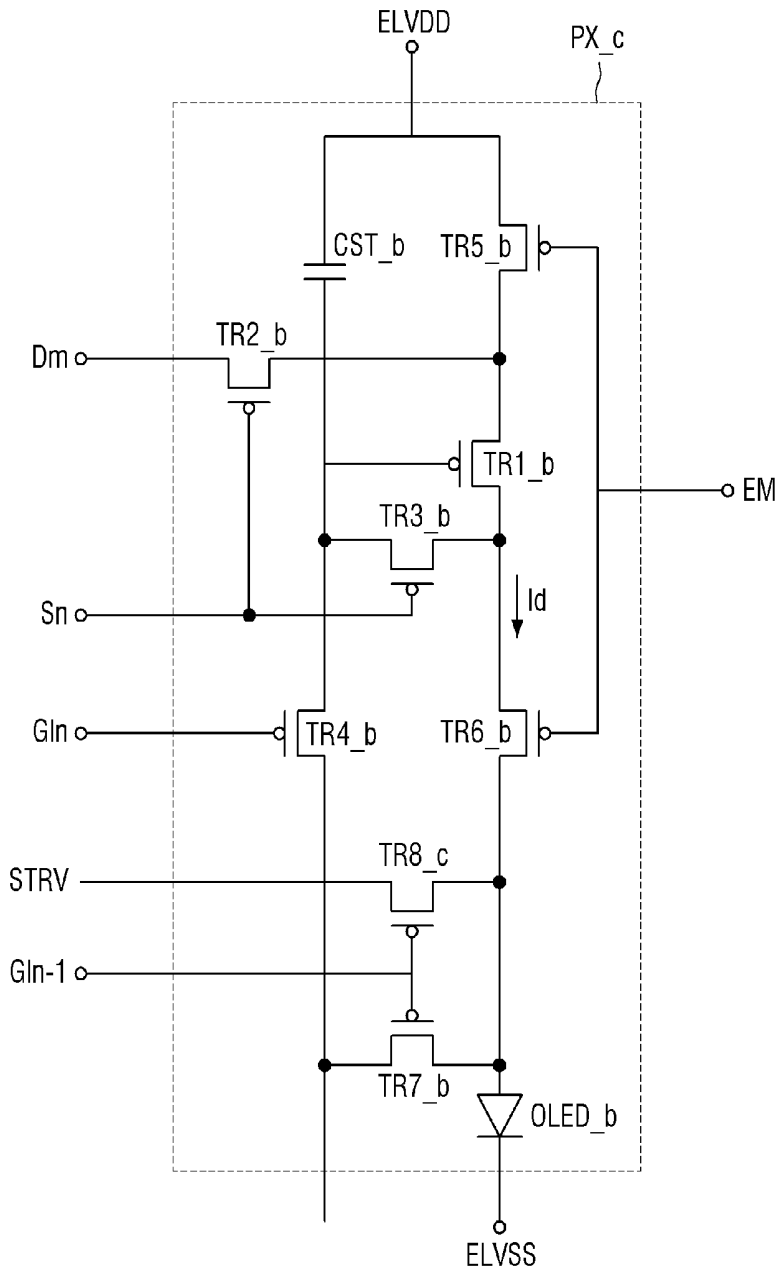

ELVDD
PX_c
CST_b
TR5_b
TR2_b
Dm
TR1_b
EM
TR3_b
Id
Sn
Gln
TR4_b
TR6_b
TR8_c
STRV
Gln-1
TR7_b
OLED_b
ELVSS

FIG.10

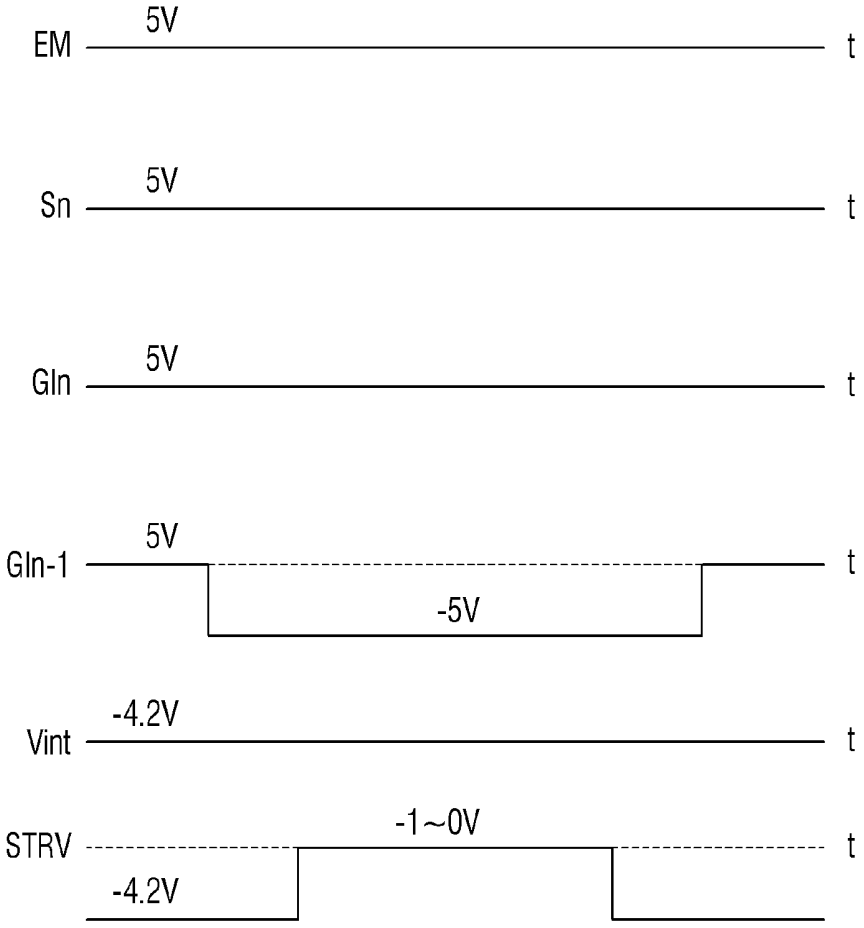
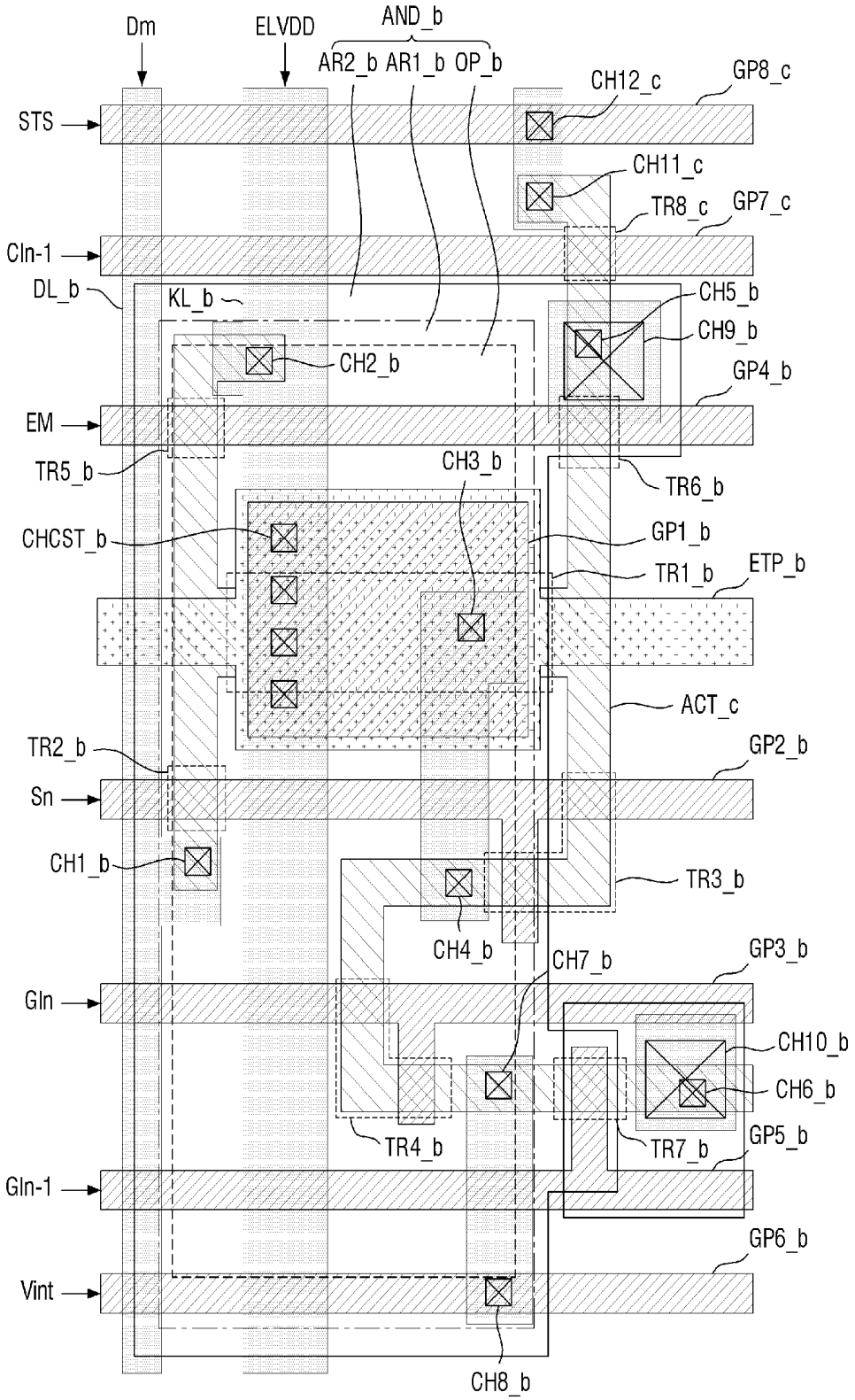


FIG.11


Dm
ELVDD
AND_b
AR2_b AR1_b OP_b
CH12_c
GP8_c
STS
CH11_c
TR8_c
GP7_c
Cln-1
DL_b
KL_b
CH5_b
CH9_b
CH2_b
GP4_b
EM
TR5_b
CH3_b
TR6_b
CHCST_b
GP1_b
TR1_b
ETP_b
ACT_c
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CH4_b
CH7_b
GP3_b
Gln
CH10_b
CH6_b
TR4_b
TR7_b
GP5_b
Gln-1
GP6_b
Vint
CH8_b

ORGANIC LIGHT-EMITTING DISPLAY DEVICE AND DRIVING METHOD THEREOF

[0001] This application claims priority to Korean Patent Application No. 10-2016-0131941, filed on Oct. 12, 2016, and all the benefits accruing therefrom under 35 U.S.C. § 119, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

1. Field

[0002] The present disclosure relates to an organic light-emitting display device and a driving method thereof.

2. Description of the Related Art

[0003] Various display devices for use in multimedia devices such as televisions (TVs), mobile phones, tablet computers, navigation systems, game machines and the like have been developed.

[0004] One such display device is an organic light-emitting display device. The organic light-emitting display device is a self-emitting display device having a wide viewing angle, excellent contrast and high response speed. The organic light-emitting display device includes an organic light-emitting diode (OLED), and electrodes for providing signals to the OLED may be formed as multilayers in order to increase the luminous efficiency of the OLED.

[0005] However, in a case where the electrodes are formed as multilayers, the display quality of the organic light-emitting display device may be lowered. Specifically, the electrodes may be disposed to cover most of the area of the OLED. To reflect light emitted from the bottom of the OLED back to the top of the OLED, the electrodes may be formed as multilayers to comprise a material capable of reflecting light. However, at the contact surfaces between pairs of adjacent layers of each of the multilayers, the amount of energy required for the movement of electrons or holes may increase, and resistance may locally increase accordingly. As a result, the display quality of the organic light-emitting display device may be lowered.

SUMMARY

[0006] Exemplary embodiments of the present disclosure provide an organic light-emitting display device capable of minimizing a decrease in display quality that may be caused by electrodes formed as multilayers.

[0007] However, exemplary embodiments of the present disclosure are not restricted to those set forth herein. The above and other exemplary embodiments of the present disclosure will become more apparent to one of ordinary skill in the art to which the present disclosure pertains by referencing the detailed description of the present disclosure given below.

[0008] According to an exemplary embodiment of the present disclosure, there is provided an organic light-emitting display device. The organic light-emitting display device comprises a substrate, a thin-film transistor (TFT) disposed on the substrate, an overcoat layer disposed on the TFT, a first electrode disposed on the overcoat layer and including a lower electrode layer, an intermediate electrode layer which is disposed on the lower electrode layer, and an upper electrode layer which is disposed on the intermediate electrode layer, an emission layer disposed on the first electrode, and a second electrode disposed on the emission layer, wherein the first electrode includes a first area in which the lower electrode layer, the intermediate electrode layer and the upper electrode layer are sequentially stacked and a second area in which the lower electrode layer and the upper electrode layer are sequentially stacked.

[0009] The organic light-emitting display device may have the intermediate electrode layer have a higher reflectivity than the lower and upper electrode layers.

[0010] The organic light-emitting display device may have the lower and upper electrode layers are transparent electrodes, and the intermediate electrode layer is a reflective electrode.

[0011] The organic light-emitting display device may have the first area is disposed to overlap with the emission layer.

[0012] The organic light-emitting display device may have a contact hole disposed to overlap with the first electrode, wherein the contact hole is disposed in the second area.

[0013] The organic light-emitting display device may have the second area is disposed to surround the first area.

[0014] The organic light-emitting display device may have the upper electrode layer is disposed to overlap with the intermediate electrode layer.

[0015] The organic light-emitting display device may have the second area is provided as multiple patterns disposed along the edges of the first area and spaced apart from one another.

[0016] The organic light-emitting display device may have the intermediate electrode layer is formed of aluminum (Al), silver (Ag), gold (Au), platinum (Pt), chromium (Cr), or an alloy thereof.

[0017] The organic light-emitting display device may have a resistance between bottom and top surfaces of the first electrode, measured from the first area, is lower than a resistance between the bottom and top surfaces of the first electrode, measured from the second area.

[0018] The organic light-emitting display device may have a pixel defining layer disposed between the first and second electrodes, wherein the emission layer is disposed in an opening of the pixel defining layer.

[0019] The organic light-emitting display device may have the first area is disposed to overlap with the opening.

[0020] According to the aforementioned and other exemplary embodiments of the present disclosure, there is provided an organic light-emitting display device. The organic light-emitting display device comprises a plurality of pixels receiving a gate signal, a data signal, an initialization control signal, a stress control signal, a first power supply voltage, a second power supply voltage, an initialization voltage and a stress voltage, wherein each of the plurality of pixels includes: a first transistor including a first terminal configured to receive the first power supply voltage and generate a driving current; a second transistor including a first terminal configured to receive the data signal, a second terminal electrically connected to a control terminal of the first transistor, and a control terminal receiving the gate signal; a storage capacitor including a first terminal configured to receive the first power supply voltage and a second terminal electrically connected to the control terminal of the first transistor; an organic light-emitting diode (OLED) including a first terminal electrically connected to the second terminal of the first transistor and a second terminal configured to receive the second power supply voltage and emit light

based on the driving current; an initialization transistor including a first terminal configured to receive the initialization voltage, a second terminal electrically connected to the first terminal of the OLED, and a control terminal configured to receive the initialization control signal; and an overloading transistor including a first terminal configured to receive the stress voltage, a second terminal electrically connected to the first terminal of the OLED, and a control terminal configured to receive the stress control signal.

[0021] The organic light-emitting display device may have the initialization control signal is a same signal as the stress control signal.

[0022] The organic light-emitting display device may have the initialization voltage and the stress voltage are simultaneously provided to the first terminal of the OLED.

[0023] The organic light-emitting display device may have the first and second transistors are turned off during a period when the initialization transistor and the overloading transistor are turned on.

[0024] The organic light-emitting display device may have the initialization voltage and the stress voltage have different levels.

[0025] The organic light-emitting display device may have the stress voltage is higher than the initialization voltage.

[0026] The organic light-emitting display device may have the stress control signal is an initialization control signal of a previous stage.

[0027] The organic light-emitting display device may have the initialization voltage is provided to the first terminal of the overloading transistor after the application of the initialization voltage and the stress voltage to the first terminal of the OLED.

[0028] Other features and exemplary embodiments may be apparent from the following detailed description, the drawings and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The above and other exemplary embodiments and features of the present disclosure will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

[0030] FIG. **1** is a block diagram of an organic light-emitting display device according to an exemplary embodiment of the present disclosure;

[0031] FIG. **2** is an equivalent circuit diagram of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **1**;

[0032] FIG. **3** is a layout view of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **1**;

[0033] FIG. **4** is a cross-sectional view taken along line I-I' of FIG. **3**;

[0034] FIG. **5** is a layout view of a pixel of an organic light-emitting display device according to another exemplary embodiment of the present disclosure;

[0035] FIG. **6** is an equivalent circuit diagram of a pixel of an organic light-emitting display device according to another exemplary embodiment of the present disclosure;

[0036] FIG. **7** is a layout view of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **6**;

[0037] FIG. **8** is a cross-sectional view taken along line II-II' of FIG. **7**;

[0038] FIG. **9** is an equivalent circuit diagram of a pixel of an organic light-emitting display device according to another exemplary embodiment of the present disclosure;

[0039] FIG. **10** is a schematic view illustrating the waveforms of signals applied to a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **9**; and

[0040] FIG. **11** is a layout view of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **9**.

DETAILED DESCRIPTION

[0041] The present inventive concept will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will filly convey the scope of the invention to those skilled in the art. The same reference numbers indicate the same components throughout the specification. In the attached figures, the thickness of layers and regions is exaggerated for clarity.

[0042] It will be understood that, although the terms first, second, third, etc., may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the teachings of the invention.

[0043] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms, including "at least one," unless the content clearly indicates otherwise. "Or" means "and/or." As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. It will be further understood that the terms "comprises" and/or "comprising," or "includes" and/or "including" when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0044] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0045] In the present inventive concept, an electronic apparatus may be any apparatus provided with a display device. Examples of the electronic apparatus may include

smart phones, mobile phones, navigators, game machines, TVs, car head units, notebook computers, laptop computers, tablet computers, personal media players (PMPs), and personal digital assistants (PDAs). The electronic apparatus may be embodied as a pocket-sized portable communication terminal having a wireless communication function. Further, the display device may be a flexible display device capable of changing its shape.

[0046] Hereinafter, embodiments of the present inventive concept will be described with reference to the attached drawings.

[0047] FIG. **1** is a block diagram of an organic light-emitting display device according to an exemplary embodiment of the present disclosure.

[0048] Referring to FIG. **1**, the organic light-emitting display device includes a scan driver **100**, a data driver **200** and a display panel DP.

[0049] The scan driver **100** receives gate control signals (not illustrated) from a timing controller (not illustrated). The gate control signals may include a vertical start signal for starting the operation of the scan driver **100** and a clock signal for determining the output timing of signals. The scan driver **100** generates a plurality of gate signals and sequentially outputs the plurality of gate signals to a plurality of gate lines GL**1** to Glen, respectively, which will be described later. The scan driver **100** generates a plurality of emission control signals in response to the gate control signals, and outputs the plurality of emission control signals to a plurality of emission lines EL**1** to ELn, respectively, which will be described later.

[0050] FIG. **1** illustrates an example in which the plurality of gate signals and the plurality of emission control signals are both output from a single scan driver, i.e., the scan driver **100**, but the present disclosure is not limited thereto. That is, in another example, a plurality of scan drivers may be provided to divide and output the plurality of gate signals and to divide and output the plurality of emission control signals. Also, in another example, a driving circuit for generating and outputting the plurality of gate signals and a driving circuit for generating and outputting the plurality of emission control signals may be separately provided.

[0051] The data driver **200** receives data control signals (not illustrated) and a plurality of image data (not illustrated) from the timing controller. The data driver **200** converts the plurality of image data into a plurality of data signals and outputs the plurality of data signals to a plurality of data lines DU to DLm, respectively, which are insulated from the gate lines GL**1** to GLn. The plurality of data signals are analog voltages corresponding to the gray levels of the plurality of image data.

[0052] The display panel DP includes the gate lines GL**1** to GLn, the emission lines EL**1** to ELn, the data lines DL**1** to DLm and a plurality of pixels PX. The gate lines GL**1** to GLn extend in a first direction DR**1** and are arranged in a second direction DR**2** that intersects the first direction DR**1**. The emission lines EL**1** to ELn may be arranged in parallel to the gate lines GL**1** to GLn, respectively. The data lines DL**1** to DLm are insulated from the gate lines GL**1** to GLn and intersect the gate lines GL**1** to GLn.

[0053] Each of the pixels PX is connected to one of the gate lines GL**1** to GLn, one of the emission lines ELI to ELn and one of the data lines DL**1** through DLm. Although not specifically illustrated in FIG. **1**, each of the pixels PX may be connected to more than one of the gate lines GL**1** through GLn.

[0054] FIG. **2** is an equivalent circuit diagram of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **1**.

[0055] Referring to FIG. **2**, a pixel PX includes an organic light-emitting diode (OLED) "OLED", a first transistor TR**1**, a second transistor TR**2** and a storage capacitor CST. The equivalent circuit of the pixel PX is not particularly limited to that illustrated in FIG. **2**, but may vary.

[0056] The first transistor TR**1** includes a control electrode, which is connected to a gate line GL, an input electrode, which is connected to a data line DL, and an output electrode. The first transistor TR**1** outputs a data signal Dm applied to the data line DL in response to a gate signal applied to the gate line GL.

[0057] The storage capacitor CST includes a first electrode, which is connected to the first transistor TR**1**, and a second electrode, which receives a first power supply voltage ELVDD. The storage capacitor CST is charged with a voltage corresponding to the data signal Dm received from the first transistor TR**1**.

[0058] The second transistor TR**2** includes a control electrode, which is connected to the output electrode of the first transistor TR**1** and the first electrode of the storage capacitor CST, an input electrode, which receives the first power supply voltage ELVDD, and an output electrode. The output electrode of the second transistor TR**2** is connected to the OLED "OLED". The second transistor TR**2** controls a driving current that flows in the OLED "OLED" to correspond with the voltage stored in the storage capacitor CST.

[0059] The OLED "OLED" includes an anode electrode AND, which is connected to the second transistor TR**2** and receives the first power supply voltage ELVDD, and a cathode electrode CTD, which receives a second power supply voltage ELVSS. The OLED "OLED" further includes an emission layer EML, which is disposed between the anode electrode AND and the cathode electrode CTD. The OLED "OLED" emits light while the second transistor TR**2** is turned on.

[0060] FIG. **3** is a layout view of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **1**, and FIG. **4** is a cross-sectional view taken along line I-I' of FIG. **3**.

[0061] The organic light-emitting display device according to the exemplary embodiment of FIG. **1** will hereinafter be described in further detail with reference to FIGS. **3** and **4**.

[0062] The display panel DP includes a base substrate BS, a buffer layer BFL, signal lines (GL and DL) and a pixel PX. The elements of the display panel DP, i.e., the base substrate BS, the buffer layer BFL, the signal lines (GL and DL) and the pixel PX, may vary depending on the type of the display panel DP.

[0063] The base substrate BS may be formed of an insulating material.

[0064] The buffer layer BFL is disposed on the base substrate BS.

[0065] The buffer layer BFL prevents impurities present in the base substrate BS from flowing into the pixel PX during the manufacture of the organic light-emitting display device. Specifically, the buffer layer BFL prevents the impurities from diffusing into a semiconductor layer SL of the pixel

PX. The impurities may be introduced from the outside of the organic light-emitting display device or may be generated by pyrolysis of the base substrate BS. The impurities may be a gas or sodium discharged from the base substrate BS. Also, the buffer layer BFL blocks moisture from flowing into the pixel PX from the outside of the organic light-emitting display device.

[0066] The signal lines (GL and DL) and the pixel PX are arranged on the buffer layer BFL. The semiconductor layer SL of a second transistor TR**2** is disposed on the buffer layer BFL. The semiconductor layer SL may comprise polysilicon or amorphous silicon formed at low temperature. The semiconductor layer SL may further comprise a metal oxide semiconductor.

[0067] The semiconductor layer SL includes a channel region, which serves as a channel through which electrons or holes can travel, and first and second ion-doped regions, which are disposed with the channel region interposed therebetween.

[0068] A gate insulating layer GI, which covers the semiconductor layer SL, is disposed on the buffer layer BFL. The gate insulating layer GI includes an organic film and/or an inorganic film. Specifically, the gate insulating layer GI may include a plurality of inorganic thin films. The plurality of inorganic thin films may include a silicon nitride layer and a silicon oxide layer,

[0069] A gate line GL is disposed on the gate insulating layer GI. A control electrode GE**1** (hereinafter, the first control electrode GE**1**) of a first transistor TR**1** and a control electrode GE**2** (hereinafter, the second control electrode GE**2**) of the second transistor TR**2** are disposed on the gate insulating layer GI.

[0070] A first electrode CE**1** of a storage capacitor CST may be disposed on the gate insulating layer GI, but the location of the first electrode CE**1** is not particularly limited. The first electrode CE**1** may be fabricated by the same photolithography process as the gate line GL. In other words, the first electrode CE**1** may be formed of the same material as the gate line GL.

[0071] An interlayer insulating layer IL, which covers the first control electrode GE**1**, the second control electrode GE**2** and the first electrode CE**1**, is disposed on the gate insulating layer GI. The interlayer insulating layer IL may include an organic film and/or an inorganic film. The interlayer insulating layer IL may include a plurality of inorganic thin films. The plurality of inorganic thin films may include a silicon nitride layer and a silicon oxide layer.

[0072] The data line DL and a power line KL are disposed on the interlayer insulating layer IL. An input electrode SE**1** (hereinafter, the first input electrode SE**1**) and an output electrode DE**1** (hereinafter, the first output electrode DE**1**) of the first transistor TR**1** are disposed on the interlayer insulating layer IL. An input electrode SE**2** (hereinafter, the second input electrode SE**2**) and an output electrode DE**2** (hereinafter, the second output electrode DE**2**) of the second transistor TR**2** are disposed on the interlayer insulating layer IL. The first input electrode SE**1** is branched off from the data line DL. The second input electrode SE**2** is branched off from the power line KL.

[0073] A second electrode CE**2** of the storage capacitor CST may be disposed on the interlayer insulating layer IL, but the location of the second electrode CE**2** is not particularly limited. The second electrode CE**2** may be fabricated by the same photolithography process as the data line DL and the power line KL and may be formed of the same material as the data line DL and the power line KL.

[0074] The first input electrode SE**1** and the first output electrode DE**1** are connected to a semiconductor layer (not illustrated) of the first transistor TR**1** via first and second contact holes CH**1** and CH**2**, which penetrate the gate insulating layer GI and the interlayer insulating layer IL. The first output electrode DE**1** is connected to the first electrode CE**1** via a third contact hole CH**3**, which penetrates the interlayer insulating layer IL. The second input electrode SE**2** and the second output electrode DE**2** are connected to the semiconductor layer SL of the second transistor TR**2** via fourth and fifth contact holes CH**4** and CH**5**, which penetrate the gate insulating layer GI and the interlayer insulating layer IL. In another exemplary embodiment, the first transistor TR**1** and the second transistor TR**2** may be configured to have a bottom gate structure.

[0075] A passivation layer PL, which covers the first input electrode SE**1**, the first output electrode DE**1**, the second input electrode SE**2** and the second output electrode DE**2**, is formed on the interlayer insulating layer IL. The passivation layer PL includes an organic film and/or an inorganic film. Specifically, the passivation layer PL may comprise an organic material to provide a planar surface.

[0076] A pixel defining layer PDL and an OLED "OLED" are disposed on the passivation layer PL. The OLED "OLED" includes an anode electrode AND, a hole transport region HTR, an emission layer EML, an electron transport region ETR and a cathode electrode CTD. The anode electrode AND is connected to the second output electrode DE**2** via a sixth contact hole CH**6**, which penetrates the passivation layer PL. The locations of the anode electrode AND and the cathode electrode CTD of the OLED "OLED" may be reversed.

[0077] The anode electrode AND is disposed on the passivation layer PL. An opening OP of the pixel defining layer PDL exposes the anode electrode AND.

[0078] The anode electrode AND may be a pixel electrode and an anode electrode, The anode electrode AND may have a multilayer structure consisting of a plurality of layers that are formed of a transparent metal oxide and a metal.

[0079] The anode electrode AND includes a lower electrode layer LL, an intermediate electrode layer ML and an upper electrode layer UL.

[0080] The lower electrode layer LL may be directly connected to the second output electrode DE**2** and may thus receive a voltage from the second output electrode DE**2**. The lower electrode layer LL may be a transmissive electrode, a transflective electrode, or a reflective electrode. In a case where the lower electrode layer LL is a transmissive electrode, the lower electrode layer LL may be formed of a transparent metal oxide such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), or indium tin zinc oxide (ITZO). In a case where the lower electrode layer LL is a transflective electrode or a reflective electrode, the lower electrode layer LL may comprise a metal such as silver (Ag), magnesium (Mg), aluminum (Al), platinum (Pt), palladium (Pd), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chromium (Cr), or a mixture thereof.

[0081] The intermediate electrode layer ML may be disposed on the lower electrode layer LL to overlap with part of the lower electrode layer LL. The intermediate electrode layer ML may reflect light emitted from the emission layer EML in an upward direction. In order to improve the

reflection efficiency of the anode electrode AND, the intermediate electrode layer ML may be formed of a metal material having a high reflection efficiency such as Al, Ag, Au, Pt, or Cr or an alloy thereof. The intermediate electrode layer ML may receive the voltage provided to the lower electrode layer LL.

[0082] The upper electrode layer UL may be disposed on the lower electrode layer LL or the intermediate electrode layer ML to overlap with the intermediate electrode layer ML. The upper electrode layer UL may receive the voltage provided to the intermediate electrode layer ML or the lower electrode layer LL. The upper electrode layer LL may be a transmissive electrode, a transflective electrode, or a reflective electrode. In a case where the upper electrode layer LL is a transmissive electrode, the upper electrode layer LL may be formed of a transparent metal oxide such as ITO, IZO, ZnO, or ITZO. In a case where the upper electrode layer LL is a transflective electrode or a reflective electrode, the upper electrode layer LL may comprise a metal such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, or a mixture thereof.

[0083] The anode electrode AND may include two areas having different stack structures, as viewed from a direction perpendicular to the top surface of the base substrate BS, i.e., the viewpoint of FIG. **3**.

[0084] Specifically, the anode electrode AND includes a first area AR**1** in which the lower electrode layer LL, the intermediate electrode layer ML and the upper electrode layer UL are sequentially stacked and a second area AR**2** in which the lower electrode layer LL and the upper electrode layer UL are sequentially stacked.

[0085] The second area AR**2** may be disposed to surround the first area AR**1**. Accordingly, the first area AR**1** can be sufficiently secured, and the second area AR**2** can also be sufficiently secured.

[0086] The upper electrode layer UL may be formed to overlap with the intermediate electrode layer ML. Accordingly, the anode electrode AND can smoothly transmit signals to the hole transport region HTR.

[0087] The first area AR**1** may be disposed to overlap with the emission layer EML. Accordingly, since the intermediate electrode layer ML, which has a high reflectivity, is disposed in the first area AR**1**, the amount of light emitted upward can be sufficiently secured.

[0088] Since the anode electrode AND includes the first and second areas AR**1** and AR**2**, the degradation of the display quality of the organic light-emitting display device can be minimized. Specifically, since the anode electrode AND is composed of three layers, resistance may increase locally near the surfaces of the three layers. That is, in areas near the surfaces of the three layers of the anode electrode AND, differences in electric potential are generated among the three layers of the anode electrode AND due to the formation of a hole injection barrier, and as a result, high resistance may be generated against the transmission of signals. However, the generation of such high resistance can be prevented because the first area AR**1** includes a total of two contact surfaces, i.e., the contact surface between the lower electrode layer LL and the intermediate electrode layer ML and the contact surface between the intermediate electrode layer ML and the upper electrode layer UL, whereas the second area AR**2** includes only one contact surface, i.e., the contact surface between the lower electrode layer LL and the upper electrode layer ML. Thus, a voltage can be smoothly transmitted by the anode electrode AND, and as a result, the display quality of the organic light-emitting display device can be improved.

[0089] The hole transport region HTR is disposed on the anode electrode AND. The hole transport region HTR may include at least one of a hole injection layer, a hole transport layer, a buffer layer and an electron blocking layer.

[0090] The hole transport region HTR may have a single-layer structure formed of a single material, a single-layer structure formed of a plurality of different materials or a multilayer structure formed of a plurality of different materials.

[0091] For example, the hole transport region HTR may have a single-layer structure formed of a plurality of different materials or may have a multilayer structure in which a hole injection layer and a hole transport layer, a hole injecting layer, a hole transport layer and a buffer layer, a hole injection layer and a buffer layer, a hole transport layer and a buffer layer, or a hole injection layer, a hole transport layer and an electron blocking layer are sequentially stacked on the anode electrode AND, but the present disclosure is not limited thereto.

[0092] The hole transport region HTR may be formed by various methods such as vacuum deposition, spin coating, casting, Langmuir-Blodgett (LB) deposition, inkjet printing, laser printing, or laser induced thermal imaging (LITI).

[0093] The emission layer EML is disposed on the hole transport region HTR. The emission layer EML may be formed by various methods such as vacuum deposition, spin coating, casting, LB deposition, inkjet printing, laser printing, or LITI.

[0094] The material of the emission layer EML is not particularly limited. For example, the emission layer EML may be formed of a material emitting red light, green light, or blue light and may comprise a fluorescent material or a phosphorescent material. The emission layer EML may include a host and a dopant.

[0095] The type of the host of the emission layer EML is not particularly limited. For example, tris(8-hydroxyquinolino)aluminum (Alq3), 4,4'-bis(N-carbazolyl)-1,1'-biphenyl (CBP), poly(n-vinylcabazole) (PVK), 9,10-di(naphthalene-2-yl)anthracene (ADN), 4,4',4"-Tris(carbazol-9-yl)-triphenylamine (TCTA), 1,3,5-tris(N-phenylbenzimidazole-2-yl) benzene (TPBi), 3-tert-butyl-9,10-di(naphth-2-yl) anthracene (TBADN), distyrylarylene (DSA), 4,4'-bis(9-carbazolyl)-2,2'-dimethyl-biphenyl (CDBP), or 2-Methyl-9, 10-bis(naphthalen-2-yl)anthracene (MADN) may be used as the host of the emission layer EML.

[0096] In a case where the emission layer EML emits red light, the emission layer EML may comprise a fluorescent material containing tris(dibenzoylmethanato)phenanthoroline europium (PBD: Eu(DBM)3(Phen)) or perylene. In a case where the emission layer EML emits red light, the dopant of the emission layer EML may be selected from a metal complex or an organometallic complex such as bis(1-phenylisoquinoline)acetylacetonate iridium (PIQIr(acac)), bis(1-phenylquinoline)acetylacetonate iridium (PQIr(acac)), tris(1-phenylquinoline)iridium (PQIr), or octaethylporphyrin platinum (PtOEP).

[0097] In a case where the emission layer EML emits green light, the emission layer EML may comprise a fluorescent material containing Alq3. In a case where the emission layer EML emits green light, the dopant of the emission

layer EML may be selected from a metal complex or an organometallic complex such as fac-tris(2-phenylpyridine) iridium (Ir(ppy)3).

[0098] In a case where the emission layer EML emits blue light, the emission layer EML may comprise a fluorescent material containing any one selected from the group consisting of spiro-DPVBi, spiro-6P, distyrylbenzene (DSB), distyryl-arylene (DSA), a polyfluorene (PFO)-based polymer and a poly(p-phenylene vinylene) (PPV)-based polymer. In a case where the emission layer EML emits blue light, the dopant of the emission layer EML may be selected from a metal complex or an organometallic complex such as, for example, (4,6-F2ppy)2Irpic.

[0099] The electron transport region ETR is disposed on the emission layer EML.

[0100] The electron transport region ETR may include at least one of a hole blocking layer, an electron transport layer and an electron injection layer, but the present disclosure is limited thereto. For example, the electron transport region ETR may have a multilayer structure in which an electron transport layer and an electron injection layer or a hole blocking layer, an electron transport layer and an electron injection layer are sequentially stacked on the emission layer EML or a single-layer structure in which two of a hole blocking layer, an electron transport layer and an electron injection layer are mixed together, but the present disclosure is not limited thereto.

[0101] The electron transport region ETR may be formed by various methods such as vacuum deposition, spin coating, casting, LB deposition, inkjet printing, laser printing, or LITI.

[0102] The cathode electrode CTD is disposed on the electron transport region ETR.

[0103] The cathode electrode CTD may be a common electrode and a cathode electrode. The cathode electrode CTD may be a transmissive electrode, a transflective electrode, or a reflective electrode. In a case where the cathode electrode CTD is a transmissive electrode, the cathode electrode CTD may comprise Li, Ca, LiF/Ca, LiF/Al, Al, Mg, BaF, Ba, Ag, or a compound or mixture thereof (for example, the mixture of Ag and Mg). The cathode electrode CTD may include an auxiliary electrode. The auxiliary electrode may include a film obtained by depositing Li, Ca, LiF/Ca, LiF/Al, Al, Mg, BaF, Ba, Ag, or a compound or mixture thereof (for example, the mixture of Ag and Mg) to face the emission layer EML and a transparent metal oxide disposed on the film and formed of, for example, ITO, IZO, ZnO, ITZO, molybdenum (Mo), or titanium (Ti). In a case where the cathode electrode CTD is a transflective or reflective electrode, the cathode electrode CTD may comprise Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, LiF/Ca, LiF/Al, Mo, Ti, or a compound or mixture thereof (for example, the mixture of Ag and Mg). In this case, the cathode electrode CTD may have a multilayer structure including a reflective or transflective film formed of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, LiF/Ca, LiF/Al, Mo, Ti, or a compound or mixture thereof (for example, the mixture of Ag and Mg) and a transparent conductive film formed of ITO, IZO, ZnO, or ITZO.

[0104] An encapsulation layer SIL is disposed on the cathode electrode CTD. The encapsulation layer SIL may include a plurality of thin film encapsulation layers. The thin film encapsulation layers may include a silicon nitride layer and a silicon oxide layer.

[0105] An organic light-emitting display device according to another exemplary embodiment of the present disclosure will hereinafter be described with reference to FIG. **5**.

[0106] FIG. **5** is a layout view of a pixel of an organic light-emitting display device according to another exemplary embodiment of the present disclosure.

[0107] The structure of an anode electrode AND_a of a pixel PX_a of FIG. **5** differs from the structure of the anode electrode AND of the pixel PX of FIG. **3**. The pixel PX_a of FIG. **5** will hereinafter be described, focusing mainly on differences with the pixel PX of FIG. **3**.

[0108] Referring to FIG. **5**, the arrangement of a first area AR_**1***a* and a second area AR_**2***a* of the anode electrode AND_a of the pixel PX_a may differ from the arrangement of the first area AR**1** and the second area AR**2** of the anode electrode AND of FIG. **3**. Specifically, the second region AR**2**_*a* may be disposed along the edges of the first region AR**1**_*a* to form a plurality of strips that are spaced apart from one another.

[0109] Due to this arrangement of the first and second areas AR**1**_*a* and AR**2**_*a*, the ratio of the second area AR**2**_*a*, which has a relatively low reflectivity, to the entire area of the anode electrode AND_a is lower than the ratio of the second area AR**2** of FIG. **3** to the entire area of the anode electrode AND of FIG. **3**. Accordingly, the reflectivity of the anode electrode AND_a may be lower than the reflectivity of the anode electrode AND.

[0110] However, the shape of the second area AR**2**_*a* is not particularly limited, and may be partially modified. For example, the second area AR**2**_*a* may have different lengths or widths from one region to another region or may be arranged to form shapes other than strips.

[0111] FIG. **6** is an equivalent circuit diagram of a pixel of an organic light-emitting display device according to another exemplary embodiment of the present disclosure.

[0112] A pixel PX_b of FIG. **6** differs from the pixel PX of FIG. **2** in that it includes more transistors than the pixel PX of FIG. **2** to be driven.

[0113] Referring to FIG. **6**, the pixel PX_b includes an OLED "OLED_b", a first transistor TR**1**_*b*, a second transistor TR**2**_*b*, a third transistor TR**3**_*b*, a storage capacitor CST_b, a fourth transistor TR**4**_*b*, a fifth transistor TR**5**_*b*, a sixth transistor TR**6**_*b* and a seventh transistor TR**7**_*b*.

[0114] The OLED "OLED_b" may emit light based on a driving current Id. The OLED "OLED_b" may include a first terminal and a second terminal. The second terminal of the OLED "OLED_b" may receive a second power supply voltage ELVSS. For example, the first terminal of the OLED "OLED_b" may be an anode terminal, and the second terminal of the OLED "OLED_b" may be a cathode terminal. In another example, the first terminal of the OLED "OLED_b" may be a cathode terminal, and the second terminal of the OLED "OLED_b" may be an anode terminal.

[0115] The second transistor TR**2**_*b* may include a gate terminal, a first terminal and a second terminal. The gate terminal of the second transistor TR**2**_*b* may receive a scan signal Sn of a current stage. The first terminal of the second transistor TR**2**_*b* may receive a data signal Dm. The second terminal of the second transistor TR**2**_*b* may be coupled to the first terminal of the first transistor TR**1**_*b*. For example, the first terminal of the second transistor TR**2**_*b* may be a source terminal, and the second terminal of the second transistor TR**2**_*b* may be a drain terminal. In another example, the first terminal of the second transistor TR**2**_*b*

may be a drain terminal, and the second terminal of the second transistor TR2_*b* may be a source terminal,

[0116] The second transistor TR2_*b* may provide the data signal Dm to the first terminal of the first transistor TR1_*b* during an active period of the scan signal Sn. In this case, the second transistor TR2_*b* may operate in a linear region.

[0117] The third transistor TR3_*b* may include a gate terminal, a first terminal and a second terminal. The gate terminal of the third transistor TR3_*b* may receive the scan signal Sn. The first terminal of the third transistor TR3_*b* may be connected to the second terminal of the first transistor TR1_*b*. The second terminal of the third transistor TR3_*b* may be connected to the gate terminal of the first transistor TR1_*b*. For example, the first terminal of the third transistor TR3_*b* may be a source terminal, and the second terminal of the third transistor TR3_*b* may be a drain terminal. In another example, the first terminal of the third transistor TR3_*b* may be a drain terminal, and the second terminal of the third transistor TR3_*b* may be a source terminal.

[0118] The third transistor TR3_*b* may connect the gate terminal and the second terminal of the first transistor TR1_*b* during the active period of the scan signal Sn. In this case, the third transistor TR3_*b* may operate in a linear region. That is, the third transistor TR3_*b* may diode-connect the first transistor TR1_*b* during the active period of the scan signal Sn. Since the first transistor TR1_*b* is diode-connected, as much a voltage difference as the threshold voltage of the first transistor TR1_*b* may be generated between the first terminal of the first transistor TR1_*b* and the gate terminal of the first transistor TR1_*b* by the threshold voltage of the first transistor TR1_*b*. As a result, a voltage obtained by adding the generated voltage difference (i.e., the threshold voltage of the first transistor TR1_*b*) to the voltage of the data signal Dm, which is provided to the first terminal of the first transistor TR1_*b* during the active period of the scan signal Sn, may be provided to the gate terminal of the first transistor TR1_*b*. That is, the data signal Dm may be compensated by as much as the threshold voltage of the first transistor TR1_*b*, and the compensated data signal Dm may be provided to the gate terminal of the first transistor TR1_*b*. Accordingly, the problem of non-uniformity in the driving current Id that may be caused by a deviation in the threshold voltage of the first transistor TR1_*b* can be addressed.

[0119] The storage capacitor CST_b may be connected between the first power supply voltage ELVDD and the gate terminal of the first transistor TR1_*b*. The storage capacitor CST_b may maintain the voltage of the gate terminal of the first transistor TR1_*b* during an inactive period of the scan signal Sn. The inactive period of the scan signal Sn may include an active period of the emission signal EM, and the driving current Id generated by the first transistor TR1_*b* during the active period of the emission signal EM may be provided to the OLED "OLED_b". Thus, the driving current Id, which is generated by the first transistor TR1_*b*, may be provided to the OLED "OLED_b" based on the voltage maintained by the storage capacitor CST_b.

[0120] The fourth transistor TR4_*b* may include a gate terminal, a first terminal and a second terminal. The gate terminal of the fourth transistor TR4_*b* may receive an initialization control signal Gln of the current stage. The first terminal of the fourth transistor TR4_*b* may receive an initialization voltage Vint. The second terminal of the fourth transistor TR4_*b* may be connected to the gate terminal of the first transistor TR1_*b*. For example, the first terminal of the fourth transistor TR4_*b* may be a source terminal, and the second terminal of the fourth transistor TR4_*b* may be a drain terminal. In another example, the first terminal of the fourth transistor TR4_*b* may be a drain terminal, and the second terminal of the fourth transistor TR4_*b* may be a source terminal.

[0121] The fourth transistor TR4_*b* may provide the initialization voltage Vint to the gate terminal of the first transistor TR1_*b* during an active period of the initialization control signal Gln. In this case, the fourth transistor TR4_*b* may operate in a linear region. That is, the fourth transistor TR4_*b* may initialize the gate terminal of the first transistor TR1_*b* to the initialization voltage Vint during the active period of the initialization control signal Gln. As a result, the initialization control signal Gln may serve as a data initialization signal.

[0122] The initialization voltage Vint may be sufficiently lower than the voltage of the data signal Dm maintained by the storage capacitor CST_b during a previous frame, and the initialization voltage Vint may be provided to the gate terminal of the first transistor TR1_*b*, which may be a p-channel metal oxide semiconductor (PMOS) transistor. Alternatively, the initialization voltage Vint may be sufficiently higher than the voltage of the data signal Dm maintained by the storage capacitor CST_b during the previous frame, and the initialization voltage Vint may be provided to the gate terminal of the first transistor TR1_*b*, which may be an n-channel metal oxide semiconductor (NMOS) transistor.

[0123] The initialization control signal Gin may be defined as being substantially the same as a scan signal Sn−1 of a previous stage. For example, the initialization control signal Gln, which is applied to an n-th row (where n is an integer of 2 or greater) of pixels among a plurality of rows of pixels included in a display panel (not illustrated), may be substantially the same as the scan signal Sn−1 previously applied to an (n−1)-th row of pixels among the plurality of rows of pixels included in the display panel. That is, the scan signal Sn−1 previously applied to the (n−1)-th row of pixels may also be applied to the n-th row of pixels. As a result, the data signal Dm may be applied to the (n−1)-th row of pixels, and at the same time, the gate terminal of the first transistor TR1_*b*, which is included in each of the n-th row of pixels, may be initialized to the initialization voltage Vint.

[0124] The fifth transistor TR5_*b* may include a gate terminal, a first terminal and a second terminal. The gate terminal of the fifth transistor TR5_*b* may receive the emission signal EM. The first terminal of the fifth transistor TR5_*b* may receive the first power supply voltage ELVDD. The second terminal of the fifth transistor TR5_*b* may be connected to the first terminal of the first transistor TR1_*b*. For example, the first terminal of the fifth transistor TR5_*b* may be a source terminal, and the second terminal of the fifth transistor TR5_*b* may be a drain terminal. In another example, the first terminal of the fifth transistor TR5_*b* may be a drain terminal, and the second terminal of the fifth transistor TR5_*b* may be a source terminal.

[0125] The fifth transistor TR5_*b* may provide the first power source voltage ELVDD to the first terminal of the first transistor TR1_*b* during the active period of the emission signal EM. On the other hand, the fifth transistor TR5_*b* may interrupt the provision of the first power supply voltage ELVDD during an inactive period of the emission signal

EM. In this case, the fifth transistor TR**5**_*b* may operate in a linear region. Specifically, the fifth transistor TR**5**_*b* provides the first power source voltage ELVDD to the first terminal of the first transistor TR**1**_*b* during the active period of the emission signal EM so that the first transistor TR**1**_*b* can generate the driving current Id. Also, the fifth transistor TR**5**_*b* interrupts the provision of the first power supply voltage ELVDD during the inactive period of the emission signal EM so that the data signal Dm, which is applied to the first terminal of the first transistor TR**1**_*b*, can be applied to the gate terminal of the first transistor TR**1**_*b*.

[0126] The sixth transistor TR**6**_*b* may include a gate terminal, a first terminal and a second terminal. The gate terminal of the sixth transistor TR**6**_*b* may receive the light emission signal EM. The first terminal of the sixth transistor TR**6**_*b* may be connected to the second terminal of the first transistor TR**1**_*b*. The second terminal of the sixth transistor TR**6**_*b* may be connected to the first terminal of the OLED "OLED_b". For example, the first terminal of the sixth transistor TR**6**_*b* may be a source terminal, and the second terminal of the sixth transistor TR**6**_*b* may be a drain terminal. In another example, the first terminal of the sixth transistor TR**6**_*b* may be a drain terminal, and the second terminal of the sixth transistor TR**6**_*b* may be a source terminal.

[0127] The sixth transistor TR**6**_*b* may provide the driving current Id, which is generated by the first transistor TR**1**_*b* during the active period of the emission signal EM, to the OLED "OLED_b". In this case, the sixth transistor TR**6**_*b* may operate in a linear region. That is, the sixth transistor TR**6**_*b* provides the driving current Id to the OLED "OLED_b" so that the OLED "OLED_b" can output light. The sixth transistor TR**6**_*b* electrically isolates the first transistor TR**1**_*b* and the OLED "OLED_b" from each other during the inactive period of the emission signal EM so that the data signal Dm (particularly, the data signal Dm compensated by as much the threshold voltage of the first transistor TR**1**_*b*) can be provided to the gate terminal of the first transistor TR**1**_*b*.

[0128] The seventh transistor TR**7**_*b* may include a gate terminal, a first terminal and a second terminal. The gate terminal of the seventh transistor TR**7**_*b* may receive an initialization control signal Gln−1 of the previous stage. The first terminal of the seventh transistor TR**7**_*b* may receive the initialization voltage Vint. The second terminal of the seventh transistor TR**7**_*b* may be connected to the first terminal of the OLED "OLED_b". For example, the first terminal of the seventh transistor TR**7**_*b* may be a source terminal, and the second terminal of the seventh transistor TR**7**_*b* may be a drain terminal. In another example, the first terminal of the seventh transistor TR**7**_*b* may be a drain terminal, and the second terminal of the seventh transistor TR**7**_*b* may be a source terminal.

[0129] The seventh transistor TR**7**_*b* may provide the initialization voltage Vint to the first terminal of the OLED "OLED_b" during an active period of the initialization control signal Gln−1. In this case, the seventh transistor TR**7**_*b* may operate in a linear region. That is, the seventh transistor TR**7**_*b* may initialize the first terminal of the OLED "OLED_b" to the initialization voltage Vint during the active period of the initialization control signal Gln−1. As a result, the initialization control signal Gln−1 can serve as a diode initialization signal.

[0130] FIG. **7** is a layout view of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **6**, and FIG. **8** is a cross-sectional view taken along line II-II' of FIG. **7**.

[0131] Referring to FIGS. **7** and **8**, a display panel DP_b includes a base substrate BS_b, a buffer layer BFP_b, active patterns ACT_b, a gate insulating layer GI_b, first through sixth gate patterns GP**1**_*b* through GP**6**_*b*, a first interlayer insulating layer IL**1**_*b*, conductive patterns ETP_b, a second interlayer insulating layer IL**2**_*b*, a data line DL_b, a first power line KL_b, a passivation layer PL_b, an OLED "OLED_b" and an encapsulation layer SIL_b.

[0132] The base substrate BS_b is formed of an insulating material.

[0133] The buffer layer BFL_b is disposed on the base substrate BS_b. The buffer layer BFL_b is almost the same as the buffer layer BFL of FIG. **4**, and thus, a detailed description thereof will be omitted.

[0134] The active patterns ACT_b are disposed on the buffer layer BFL_b. The active patterns ACT_b may comprise silicon or a semiconductor oxide including a binary compound ABx, a ternary compound (ABxCy), or a quaternary compound (ABxCyDz) containing indium (In), zinc (Zn), gallium (Ga), tin (Sn), Ti, Al, hafnium (Hf), zirconium (Zr), or magnesium (Mg). These may be used alone or in any mixture thereof.

[0135] The active patterns ACT_b may have regions doped with a high concentration of impurities to have a high electric conductivity. Accordingly, the active patterns ACT_b may form the first through seventh transistors TR**1**_*b* through TR**7**_*b*.

[0136] The gate insulating layer GI_b is disposed to cover the active patterns ACT_b. The gate insulating layer GI_b is almost the same as the gate insulating layer GI of FIG. **4**, and thus, a detailed description thereof will be omitted.

[0137] The first through sixth gate patterns GP**1**_*b* through GP**6**_*b* are disposed on the gate insulating layer GI_b. The first through sixth gate patterns GP**1**_*b* through GP**6**_*b* may comprise a metal, an alloy, a metal nitride, a conductive metal oxide, or a transparent conductive material. For example, the first through sixth gate patterns GP**1**_*b* through GP**6**_*b* may be formed of a metal such as Al, Ag, tungsten (W), copper (Cu), Ni, Cr, Mo, Ti, Pt, tantalum (Ta), Nd, scandium (Sc), or an alloy or a conductive nitride thereof. The first through sixth gate patterns GP**1**_*b* through GP**6**_*b* may also comprise any one of strontium ruthenium oxide (SrRuxOy), zinc oxide (ZnOx), ITO, tin oxide (SnOx), indium oxide (InOx), gallium oxide (GaOx), or IZO.

[0138] The first gate pattern GP**1**_*b* may overlap with the active patterns ACT_b to form the first transistor TR**1**_*b*. The first transistor TR**1**_*b* may generate the driving current Id of FIG. **6**, which is provided to the OLED "OLED_b" of FIG. **6**, and the OLED "OLED_b" may emit light based on the driving current Id.

[0139] The second gate pattern GP**2**_*b* may overlap with the active patterns ACT_b to form the second and third transistors TR**2**_*b* and TR**3**_*b*. The scan signal Sn may be provided to the second gate pattern GP**2**_*b*.

[0140] The third gate pattern GP**3**_*b* may overlap with the active patterns ACT_b to form the fourth transistor TR**4**_*b*. The initialization control signal Gln may be provided to the third gate pattern GP**3**_*b*.

[0141] The fourth gate pattern GP**4**_*b* may overlap with the active patterns ACT_b to form the fifth and sixth

transistors TR5_*b* and TR6_*b*. The emission signal EM may be provided to the fourth gate pattern GP4_*b*.

[0142] The fifth gate pattern GP5_*b* may overlap with the active patterns ACT_b to form the seventh transistor TR7_*b*. The initialization control signal Gln−1 may be provided to the fifth gate pattern GP5_*b*.

[0143] The initialization voltage Vint may be provided to the sixth gate pattern GP6_*b*.

[0144] The first interlayer insulating layer IL1_*b* is disposed on the first through sixth gate patterns GP1_*b* through GP6_*b*. The first interlayer insulating layer IL1_*b* includes an organic film and/or an inorganic film. Specifically, the first interlayer insulating layer IL1_*b* may include a plurality of inorganic thin films. The plurality of inorganic thin films may include a silicon nitride layer and a silicon oxide layer.

[0145] The conductive patterns ETP_b are disposed on the first interlayer insulating layer IL1_*b*. The conductive patterns ETP_b may be disposed to overlap with the first gate pattern GP1_*b*. Accordingly, the conductive patterns ETP_B and the first gate pattern GP1_*b* may form the storage capacitor CST_b of FIG. **6** together.

[0146] The conductive patterns ETP_b may comprise a metal alloy, a metal nitride, a conductive metal oxide, or a transparent conductive material These may be used alone or in any mixture thereof.

[0147] The second interlayer insulating layer IL2_*b* is disposed on the conductive patterns ETP_b. The second interlayer insulating layer IL2_*b*, like the first interlayer insulating layer IL1_*b*, includes an organic film and/or an inorganic film.

[0148] The data line DL_b and the first power line KL_b are disposed on the second interlayer insulating layer IL2_*b*. The data line DL_b may receive the data signal Dm. The first power line KL_b may receive the first power supply voltage ELVDD.

[0149] The passivation layer PL_b is disposed on the data line DL_b and the first power line KL_b. The passivation layer PL_b is almost the same as the passivation layer PL of FIG. **4**, and thus, a detailed description thereof will be omitted.

[0150] The anode electrode AND_b is disposed on the passivation layer PL_b. An opening OP_b of a pixel defining layer PL_b exposes the anode electrode AND_b.

[0151] The anode electrode AND_b may be a pixel electrode and an anode electrode. The anode electrode AND_b may have a multilayer structure consisting of a plurality of layers that are formed of a transparent metal oxide and a metal.

[0152] The anode electrode AND_b includes two areas having different stack structures, as viewed from a direction perpendicular to the top surface of the base substrate BS_b, i.e., the viewpoint of FIG. **7**.

[0153] The anode electrode AND_b includes a first area AR1_*b* in which a lower electrode layer LL_b, an intermediate electrode layer ML_b and an upper electrode layer UL_b are sequentially stacked and a second area AR2_*b* in which the lower electrode layer LL_b and the upper electrode layer UL_b are sequentially stacked.

[0154] The second area AR2_*b* may be disposed to surround the first area AR1_*b*. Accordingly, the first area AR1_*b* can be sufficiently secured, and the second area AR2_*b* can also be sufficiently secured.

[0155] The upper electrode layer UL_b may be formed to overlap with the intermediate electrode layer ML_b. Accordingly, the anode electrode AND_b can smoothly transmit signals to a hole transport region HTR_b.

[0156] The first region AR1_*b* may be disposed to overlap with an emission layer EML_b. Accordingly, since the intermediate electrode layer ML_b, which has a high reflectivity, is disposed in the first area AR1_*b*, the amount of light emitted upward can be sufficiently secured.

[0157] Since the anode electrode AND b includes the first and second areas AR1_*b* and AR2_*b*, the degradation of the display quality of the organic light-emitting display device can be minimized. Specifically, since the anode electrode AND_b is composed of three layers, resistance may increase locally near the surfaces of the three layers. That is, in areas near the surfaces of the three layers of the anode electrode AND_b, differences in electric potential are generated among the three layers of the anode electrode AND due to the formation of a hole injection barrier, and as a result, high resistance may be generated against the transmission of signals. However, the generation of such high resistance can be prevented because the second area AR2_*b* includes a total of two contact surfaces, i.e., the contact surface between the lower electrode layer LL_b and the intermediate electrode layer ML_b and the contact surface between the intermediate electrode layer ML_b and the upper electrode layer UL_b, whereas the first area AR includes only one contact surface, i.e., the contact surface between the lower electrode layer LL_b and the upper electrode layer ML_b. Thus, a voltage can be smoothly transmitted by the anode electrode AND_b, and as a result, the display quality of the organic light-emitting display device can be improved.

[0158] The anode electrode AND_b is almost the same as the anode electrode AND of FIG. **4**, and thus, a detailed description thereof will be omitted.

[0159] The hole transport region HTR_b is disposed on the anode electrode AND_b. The hole transport region HTR_b is almost the same as the hole transport region HTR of FIG. **4**, and thus, a detailed description thereof will be omitted.

[0160] The emission layer EML_b is disposed on the hole transport region HTR_b. The emission layer EML_b is almost the same as the emission layer EML of FIG. **4**, and thus, a detailed description thereof will be omitted.

[0161] An electron transport region ETR_b is disposed on the emission layer EML_b. The electron transport region ETR_b is almost the same as the electron transport region ETR of FIG. **4**, and thus, a detailed description thereof will be omitted.

[0162] A cathode electrode CTD_b is disposed on the electron transport region ETR_b. The cathode electrode CTD_b is almost the same as the cathode electrode CTD of FIG, **4**, and thus, a detailed description thereof will be omitted.

[0163] The encapsulation layer SIL_b is disposed on the cathode electrode CTD_b. The encapsulation layer SIL_b is almost the same as the encapsulation layer SIL of FIG. **4**, and thus, a detailed description thereof will be omitted. For connection of various wiring layers illustrated in FIG. **7**, first through ninth contact holes CH1_*b* through CH9_*b* are provided, and as a result, the first through seventh transistors TR1_*b* through TR7_*b* can operate properly.

[0164] FIG. **9** is an equivalent circuit diagram of a pixel of an organic light-emitting display device according to another exemplary embodiment of the present disclosure.

[0165] A pixel PX_c of FIG. **9** differs from the pixel PX_b of FIG. **6** in that it further includes an eighth transistor TR**8**_*c*. The pixel PX_c of FIG. **9** will hereinafter be described, focusing mainly on differences with the pixel PX_b of FIG. **6**.

[0166] Referring to FIG. **9**, the pixel PX_c includes the eighth transistor TR**8**_*c*.

[0167] The eighth transistor TR**8**_*c* may provide a stress voltage STRV to a first terminal of an OLED "OLED_b" during an active period of an initialization control signal Gln−1 of a previous stage. In this case, the eighth transistor TR**8**_*c* may operate in a linear region. That is, the eighth transistor TR**8**_*b* may provide the stress voltage STRV to the first terminal of the OLED "OLED_b" during the active period of the initialization control signal Gln−1.

[0168] Accordingly, an initialization voltage Vint, which is provided by the seventh transistor TR**7**_*b*, and the stress voltage STRV, which is provided by the eighth transistor TR**8**_*c*, can be simultaneously provided to the first terminal of the OLED "OLED_b", i.e., the anode electrode AND_b of FIG. **11**. Thus, two different voltages can be simultaneously provided to the anode electrode AND_b of the OLED "OLED_b". As a result, the anode electrode AND_b of the OLED "OLED_b" can be overloaded by the difference between the initialization voltage Vint and the stress voltage STRV. Accordingly, since the anode electrode AND_b of FIG. **11** is composed of three layers, a hole injection barrier can be eliminated from areas near the surfaces of the three layers of the anode electrode AND_b. Therefore, the resistance of the OLED "OLED_b" can be reduced, and as a result, the display quality of the organic light-emitting display device can be improved.

[0169] The organic light-emitting display device according to the exemplary embodiment of FIG. **9** will hereinafter be described in further detail with reference to FIG. **10**.

[0170] FIG. **10** is a schematic view illustrating the waveforms of signals applied to a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **9**.

[0171] Specifically, FIG. **10** illustrates the voltages of signals applied to the anode electrode AND_b of the OLED "OLED_b" of FIG. **9** while the anode electrode AND_b is being overloaded by the difference between the initialization voltage Vint and the stress voltage STRV.

[0172] Referring to FIG. **10**, the emission signal EM, the scan signal Sn, and the initialization control signal Gln all maintain an off-level voltage during the active period of the initialization control signal Gln−1.

[0173] In response to the initialization control signal Gln−1 being activated, the seventh and eighth transistors TR**7**_*b* and TR**8**_*c* of FIG. **9** are turned on so that the initialization voltage Vint and the stress voltage STRV can both be provided to the anode electrode AND_b of the OLED "OLED_b" of FIG. **9**. During the active period of the initialization control signal Gln−1, the initialization voltage Vint is −4.2V, and the stress voltage STRV is −1V to 0V. As a result, a voltage difference is generated in the OLED "OLED_b" of FIG. **11**. Due to the generated voltage difference, the anode electrode AND_b is overloaded, and as a result, the display quality of the organic light-emitting display device is improved.

[0174] The aforementioned process of overloading the anode electrode AND_b may be performed in a testing stage immediately after the fabrication of the organic light-emitting display device. After the overloading of the anode electrode AND_b, the initialization voltage Vint may be provided to the line to which the stress voltage STRV is applied, and the seventh and eighth transistors TR**7**_*b* and TR**8**_*c* of FIG. **9** may operate in the same manner.

[0175] FIG. **11** is a layout view of a pixel of the organic light-emitting display device according to the exemplary embodiment of FIG. **9**.

[0176] The pixel of FIG. **11** differs from the pixel of FIG. **7** in that it further includes seventh and eighth gate patterns GP**7**_*c* and GP**8**_*c* and the eighth transistor TR**8**_*c*. The pixel of FIG. **11** will hereinafter be described, focusing mainly on differences with the pixel of FIG. **7**.

[0177] Referring to FIG. **11**, the seventh gate pattern GP**7**_*c* may overlap with the active patterns ACT_b to form the eighth transistor TR**8**_*c*. The initialization control signal Gln-**1** may be provided to the seventh gate pattern GP**7**_*c*.

[0178] The stress voltage STRV may be provided to the eighth gate pattern GP**8**_*c*. The stress voltage STRV provided to the eighth gate pattern GP**8**_*c* may be provided to the active patterns ACT_b via eleventh and twelfth contact holes CH**11**_*c* and CH**12**_*c* and may also be provided to the anode electrode AND_b of the OLED "OLED_b" via the eighth transistor TR**8**_*c*.

[0179] However, the effects of the inventive concept are not restricted to the one set forth herein. The above and other effects of the inventive concept will become more apparent to one of daily skill in the art to which the inventive concept pertains by referencing the claims.

What is claimed is:

1. An organic light-emitting display device, comprising:

a substrate;

a thin-film transistor (TFT) disposed on the substrate;

an overcoat layer disposed on the TFT;

a first electrode disposed on the overcoat layer and including a lower electrode layer, an intermediate electrode layer which is disposed on the lower electrode layer, and an upper electrode layer which is disposed on the intermediate electrode layer;

an emission layer disposed on the first electrode; and

a second electrode disposed on the emission layer,

wherein the first electrode includes a first area in which the lower electrode layer, the intermediate electrode layer and the upper electrode layer are sequentially stacked and a second area in which the lower electrode layer and the upper electrode layer are sequentially stacked,

wherein the lower electrode layer is in direct contact with the upper electrode layer in the second area.

2. The organic light-emitting display device of claim **1**, wherein the intermediate electrode layer has a higher reflectivity than the lower and upper electrode layers.

3. The organic light-emitting display device of claim **2**, wherein

the lower and upper electrode layers are transparent electrodes, and

the intermediate electrode layer is a reflective electrode.

4. The organic light-emitting display device of claim **1**, wherein the first area is disposed to overlap with the emission layer.

5. The organic light-emitting display device of claim **1**, wherein the overcoat layer further comprising a contact hole disposed to overlap with the first electrode,

wherein the TFT and the first electrode are electrically connected through the contact hole, and

wherein the contact hole is disposed in the second area.

6. The organic light-emitting display device of claim **1**, wherein the second area is disposed to surround the first area.

7. The organic light-emitting display device of claim **6**, wherein the upper electrode layer is disposed to overlap with the intermediate electrode layer.

8. The organic light-emitting display device of claim **1**, wherein the second area is provided as multiple patterns disposed along the edges of the first area and spaced apart from one another.

9. The organic light-emitting display device of claim **1**, wherein the intermediate electrode layer is formed of aluminum (Al), silver (Ag), gold (Au), platinum (Pt), chromium (Cr), or an alloy thereof.

10. The organic light-emitting display device of claim **1**, further comprising:

a pixel defining layer disposed between the first and second electrodes,

wherein the emission layer is disposed in an opening of the pixel defining layer.

11. The organic light-emitting display device of claim **9**, wherein the first area is disposed to overlap with the opening.

12. The organic light-emitting display device of claim **12**, wherein the second area is not disposed to overlap with the opening.

13. An organic light-emitting display device, comprising:

a plurality of pixels receiving a gate signal, a data signal, an initialization control signal, a stress control signal, a first power supply voltage, a second power supply voltage, an initialization voltage and a stress voltage,

wherein each of the plurality of pixels includes: a first transistor including a first terminal configured to receive the first power supply voltage and generate a driving current; a second transistor including a first terminal configured to receive the data signal, a second terminal electrically connected to a control terminal of the first transistor, and a control terminal receiving the gate signal; a storage capacitor including a first terminal configured to receive the first power supply voltage and a second terminal electrically connected to the control terminal of the first transistor; an organic light-emitting diode (OLED) including a first terminal electrically connected to the second terminal of the first transistor and a second terminal configured to receive the second power supply voltage and emit light based on the driving current; an initialization transistor including a first terminal configured to receive the initialization voltage, a second terminal electrically connected to the first terminal of the OLED, and a control terminal configured to receive the initialization control signal; and an overloading transistor including a first terminal configured to receive the stress voltage, a second terminal electrically connected to the first terminal of the OLED, and a control terminal configured to receive the stress control signal.

14. The organic light-emitting display device of claim **13**, wherein the initialization control signal is a same signal as the stress control signal.

15. The organic light-emitting display device of claim **14**, wherein the initialization voltage and the stress voltage are simultaneously provided to the first terminal of the OLED.

16. The organic light-emitting display device of claim **13**, wherein the first and second transistors are turned off during a period when the initialization transistor and the overloading transistor are turned on.

17. The organic light-emitting display device of claim **13**, wherein the initialization voltage and the stress voltage have different levels.

18. The organic light-emitting display device of claim **17**, wherein the stress voltage is higher than the initialization voltage.

19. The organic light-emitting display device of claim **13**, wherein the stress control signal is an initialization control signal of a previous stage.

20. The organic light-emitting display device of claim **13**, wherein the initialization voltage is provided to the first terminal of the overloading transistor after the application of the initialization voltage and the stress voltage to the first terminal of the OLED.

* * * * *

专利名称(译)	有机发光显示装置及其驱动方法		
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[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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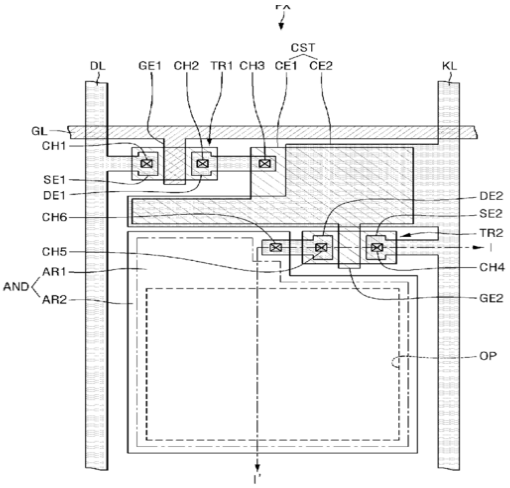
摘要(译)

提供了一种有机发光显示装置。有机发光显示装置包括基板，设置在基板上的薄膜晶体管（TFT），设置在TFT上的外涂层，设置在外涂层上并包括下电极层的第一电极，中间电极其布置在所述下电极层上，以及布置在所述中间电极层上的上电极层，布置在所述第一电极上的发射层以及布置在所述发射层上的第二电极，其中，所述第一电极包括第一区域，其中下电极层，中间电极层和上电极层被顺序地堆叠;以及第二区域，其中下电极层和上电极层被顺序地堆叠。